4-Mbit (512K x 8) Static RAM

Features

- **Very high speed**
  - **— 45 ns**
- **Voltage range: 4.5V–5.5V**
- **Pin-compatible with CY62148B**
- **Ultra low standby power**
  - **— Typical standby current: 1 μA**
  - **— Maximum standby current: 7 μA (Industrial)**
- **Ultra-low active power**
  - **— Typical active current: 2.0 mA @ f = 1 MHz**
- **Easy memory expansion with $\overline{CE}$, and $\overline{OE}$ features**
- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**
- **Available in Pb-free 32-pin SOIC and 32-pin TSOP II packages**

Functional Description[1]

The CY62148E is a high-performance CMOS static RAM organized as 512K words by 8 bits. This device features advanced circuit design to provide ultra-low active current. This is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device also has an automatic power-down feature that significantly reduces power consumption when addresses are not toggling. The device can be put into standby mode reducing power consumption by more than 99% when deselected ($\overline{CE}$ HIGH).

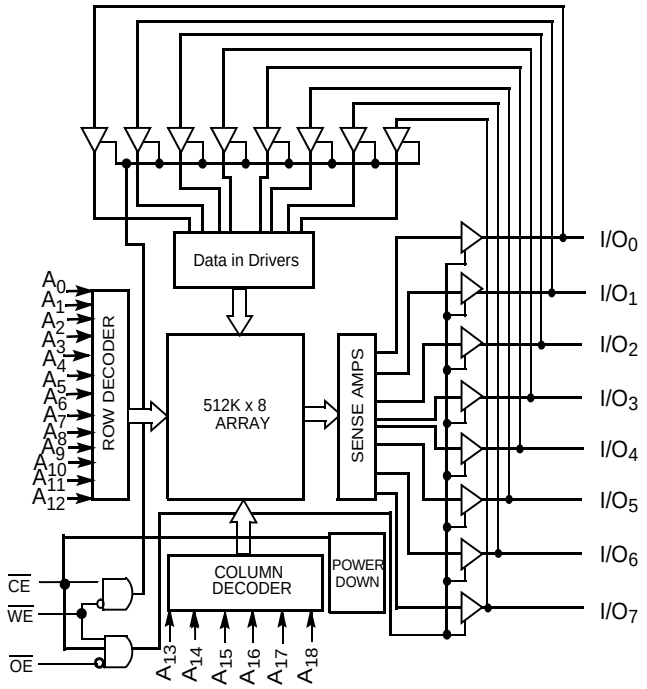
To write to the device, take Chip Enable ($\overline{CE}$) and Write Enable ($\overline{WE}$) inputs LOW. Data on the eight I/O pins (I/O_0 through I/O_7) is then written into the location specified on the address pins (A_0 through A_{18}).

To read from the device, take Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) LOW while forcing Write Enable ($\overline{WE}$) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The eight input/output pins (I/O_0 through I/O_7) are placed in a high-impedance state when the device is deselected ($\overline{CE}$ HIGH), the outputs are disabled ($\overline{OE}$ HIGH), or during a write operation ($\overline{CE}$ LOW and $\overline{WE}$ LOW).

The CY62148E is available in 32-pin SOIC and 32-pin TSOP II packages.

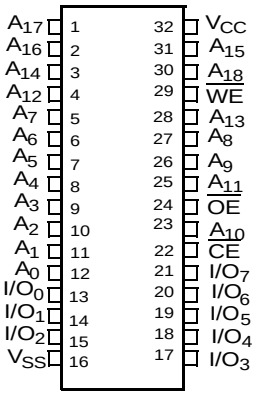
Logic Block Diagram



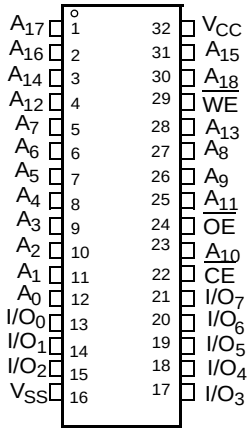
Note:
1. For best practice recommendations, please refer to the Cypress application note “System Design Guidelines” on http://www.cypress.com.

Pin Configuration[2]

32-pin SOIC Pinout
Top View



32-pin TSOP II Pinout
Top View



Product Portfolio

Product	V_{CC} Range (V)			Speed (ns)	Power Dissipation					
					Operating I_{CC} (mA)				Standby I_{SB2} (µA)	
					f = 1MHz		f = f_{max}			
	Min.	Typ.[3]	Max.		Typ.[3]	Max.	Typ.[3]	Max.	Typ.[3]	Max.
CY62148E-45LL	4.5	5.0	5.5	45 ns	2	2.5	15	20	1	7
CY62148E-55LL[4]	4.5	5.0	5.5	55 ns	2	3	15	25	1	20

Shaded areas contain preliminary information.

Notes:
2. NC pins are not connected on the die.
3. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ.)}$, $T_A = 25°C$.
4. Automotive product information is Preliminary.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....–65°C to + 150°C

Ambient Temperature with Power Applied.....–55°C to + 125°C

Supply Voltage to Ground Potential .....–0.5V to 6.0V (V_{CCMAX} + 0.5V)

DC Voltage Applied to Outputs in High-Z State[5,6].....–0.5V to 6.0V ($V_{CC\ MAX}$ + 0.5V)

DC Input Voltage[5,6] .....–0.5V to 6.0V ($V_{CC\ MAX}$ + 0.5V)

Output Current into Outputs (LOW)..... 20 mA

Static Discharge Voltage.....> 2001V (per MIL-STD-883, Method 3015)

Latch-up Current.....> 200 mA

Operating Range

Device	Range	Ambient Temperature	V_{CC}[8]	Speed
CY62148E	Industrial	–40°C to +85°C	4.5V to 5.5V	45 ns
	Automotive	–40°C to +125°C		55 ns

Electrical Characteristics (Over the Operating Range)

Parameter	Description	Test Conditions		45 ns (Industrial) Min.	45 ns (Industrial) Typ.[3]	45 ns (Industrial) Max.	55 ns (Automotive) Min.	55 ns (Automotive) Typ.[3]	55 ns (Automotive) Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –1 mA	V_{CC} = 4.5V	2.4			2.4			V
V_{OL}	Output LOW Voltage	I_{OL} = 2.1 mA	V_{CC} = 4.5V			0.4			0.4	V
V_{IH}	Input HIGH Voltage	V_{CC} = 4.5V to 5.5V		2.2		V_{CC} + 0.5	2.2		V_{CC} + 0.5	V
V_{IL}	Input LOW voltage	V_{CC} = 4.5V to 5.5V		–0.5		0.8	–0.5		0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}		–1		+1	–4		+4	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled		–1		+1	–4		+4	µA
I_{CC}	V_{CC} Operating Supply Current	f = f_{MAX} = $1/t_{RC}$	V_{CC} = V_{CCmax} I_{OUT} = 0 mA CMOS levels		15	20		15	25	mA
		f = 1 MHz			2	2.5		2	3	
I_{SB2}	Automatic CE Power-down Current — CMOS Inputs	$\overline{CE}$ ≥ V_{CC} – 0.2V V_{IN} ≥ V_{CC} – 0.2V or V_{IN} ≤ 0.2V, f = 0, V_{CC} = V_{CCmax}			1	7		1	20	µA

Capacitance (For All Packages)[8]

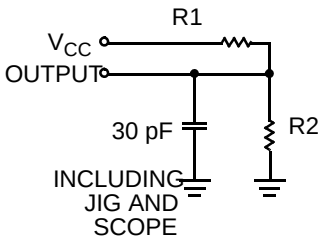
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = $V_{CC(typ)}$	10	pF
C_{OUT}	Output Capacitance		10	pF

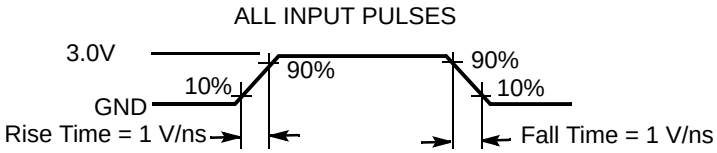
Thermal Resistance[8]

Parameter	Description	Test Conditions	SOIC Package	TSOP II Package	Unit
Θ_{JA}	Thermal Resistance (Junction to Ambient)[8]	Still Air, soldered on a 3 × 4.5 inch, 2-layer printed circuit board	75	77	°C/W
Θ_{JC}	Thermal Resistance (Junction to Case)[8]		10	13	°C/W

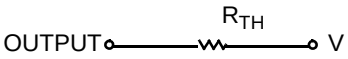
Notes:
5. $V_{IL(min.)}$ = –2.0V for pulse durations less than 20 ns for I ≤ 30 mA.
6. $V_{IH(max)}$ = V_{CC}+0.75V for pulse durations less than 20 ns.
7. Full device AC operation assumes a minimum of 100 µs ramp time from 0 to V_{CC}(min) and 200 µs wait time after V_{CC} stabilization.
8. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms





Equivalent to: THEVENIN EQUIVALENT



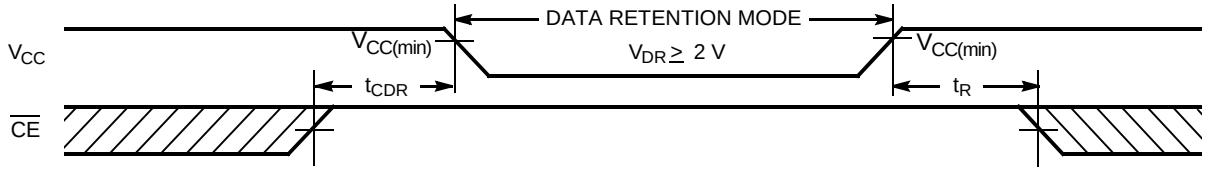
Parameters	5.0V	Unit
R1	1800	Ω
R2	990	Ω
R_{TH}	639	Ω
V_{TH}	1.77	V

Data Retention Characteristics (Over the Operating Range)

Parameter	Description	Conditions		Min.	Typ.[3]	Max.	Unit
V_{DR}	V_{CC} for Data Retention			2			V
I_{CCDR}	Data Retention Current	V_{CC}= V_{DR} $\overline{CE} \geq V_{CC} - 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$	Ind'l		1	7	µA
			Auto		1	20	
t_{CDR}[8]	Chip Deselect to Data Retention Time			0			ns
t_R[9]	Operation Recovery Time			t_{RC}			ns

Shaded areas contain preliminary information.

Data Retention Waveform



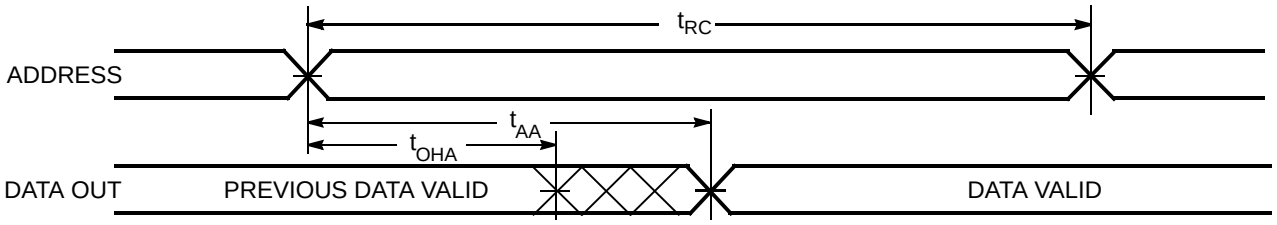
Note:
9. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min.)} \geq 100$ µs or stable at $V_{CC(min.)} \geq 100$ µs.

Switching Characteristics (Over the Operating Range)[10]

Parameter	Description	45 ns (Industrial)		55 ns (Automotive)		Unit
		Min.	Max.	Min.	Max.	
Read Cycle						
t_{RC}	Read Cycle Time	45		55		ns
t_{AA}	Address to Data Valid		45		55	ns
t_{OHA}	Data Hold from Address Change	10		10		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		45		55	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		22		25	ns
t_{LZOE}	$\overline{OE}$ LOW to LOW Z[11]	5		5		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[11, 12]		18		20	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[11]	10		10		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[11, 12]		18		20	ns
t_{PU}	$\overline{CE}$ LOW to Power-up	0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-down		45		55	ns
Write Cycle[13]						
t_{WC}	Write Cycle Time	45		55		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	35		35		ns
t_{AW}	Address Set-up to Write End	35		35		ns
t_{HA}	Address Hold from Write End	0		0		ns
t_{SA}	Address Set-up to Write Start	0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	35		35		ns
t_{SD}	Data Set-up to Write End	25		25		ns
t_{HD}	Data Hold from Write End	0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High-Z[11, 12]		18		20	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low-Z[11]	10		10		ns

Switching Waveforms

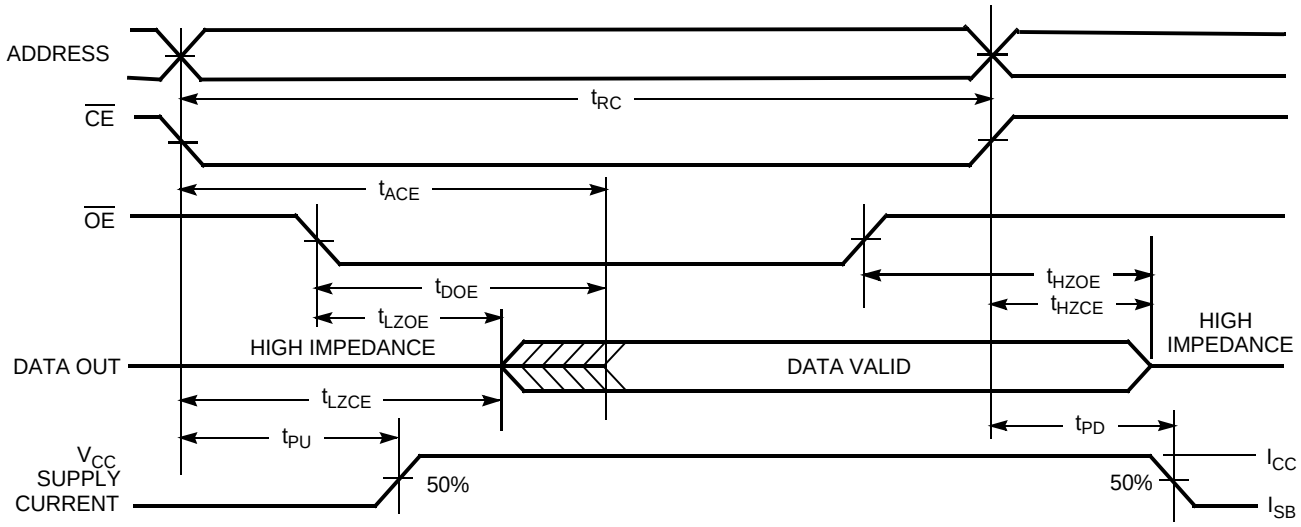
Read Cycle 1 (Address Transition Controlled)[14,15]



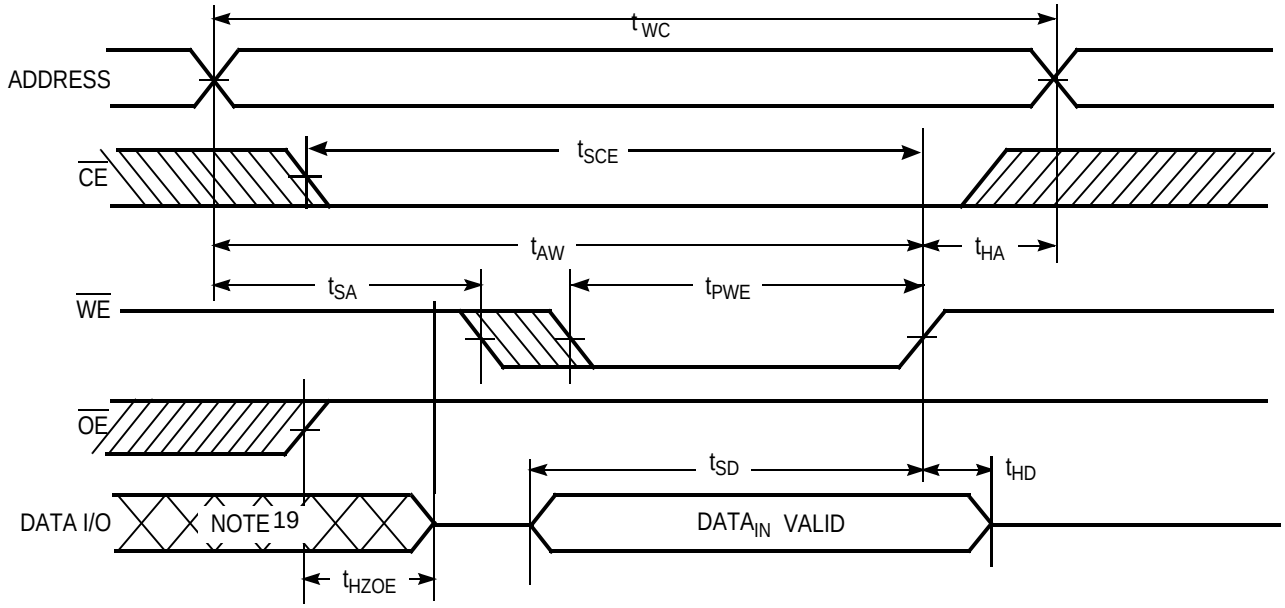
Notes:
10. Test conditions for all parameters other than tri-state parameters assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3V, and output loading of the specified I_{OL}/I_{OH} as shown in the "AC Test Loads and Waveforms" section.
11. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
12. t_{HZOE}, t_{HZCE}, and t_{HZWE} transitions are measured when the outputs enter a high-impedance state.
13. The internal Write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}$ = V_{IL}. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input set-up and hold timing should be referenced to the edge of the signal that terminates the write.
14. The device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}.
15. $\overline{WE}$ is HIGH for read cycle.

Switching Waveforms (continued)

Read Cycle No. 2 (OE Controlled)[15,16]



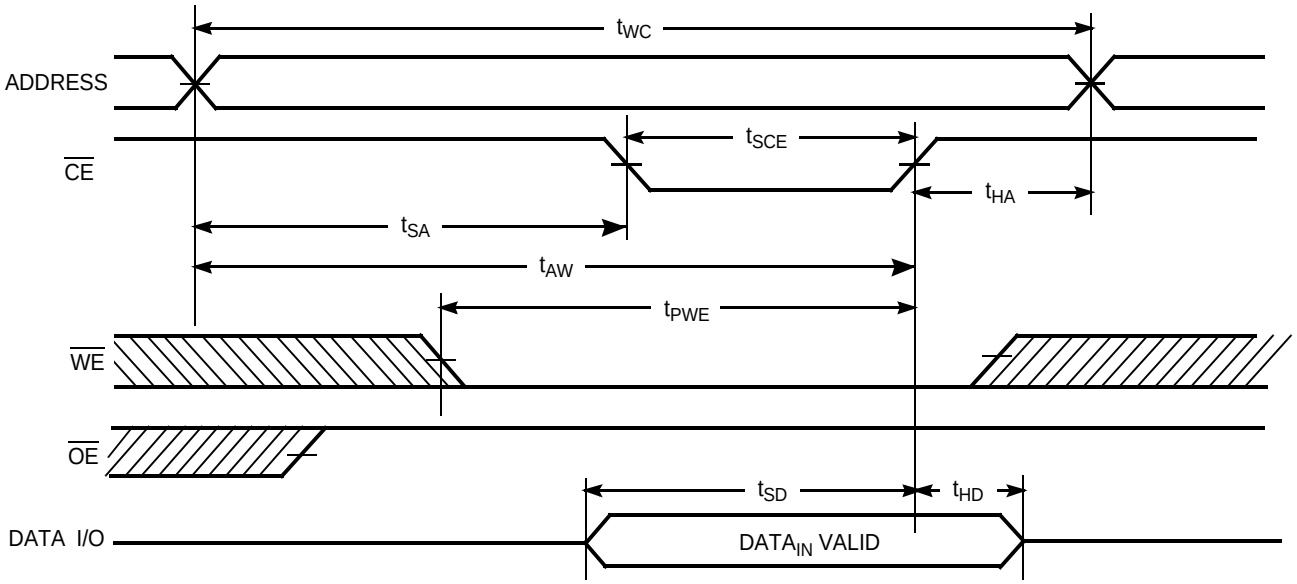
Write Cycle No. 1(WE Controlled)[13,17,18]



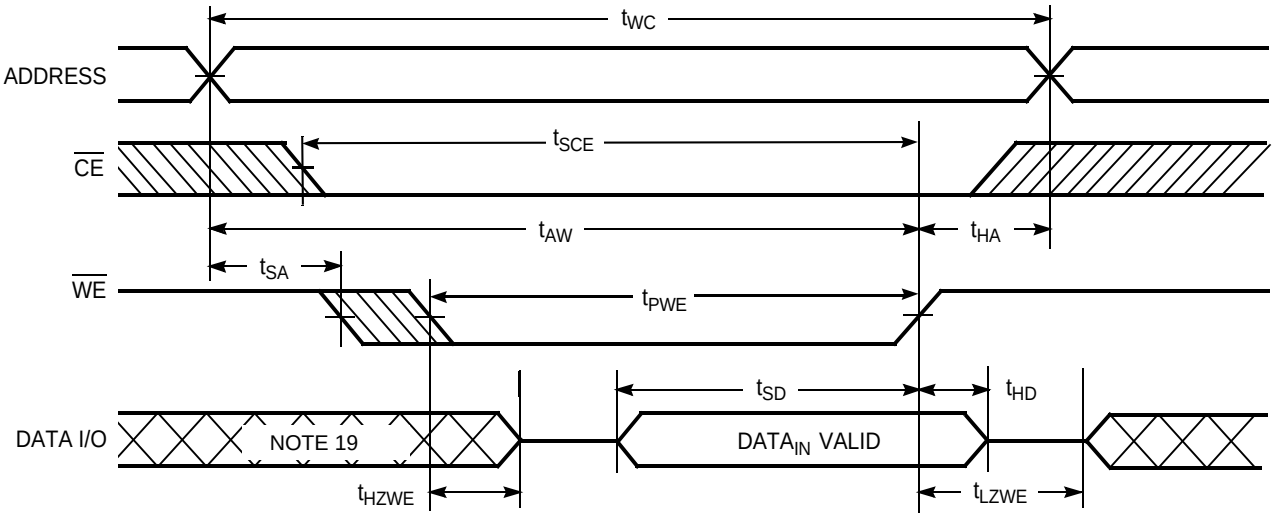
Notes:
16. Address valid prior to or coincident with CE transition LOW.
17. Data I/O is high impedance if OE = V_{IH}.
18. If CE goes HIGH simultaneously with WE = V_{IH}, the output remains in a high-impedance state.
19. During this period, the I/Os are in output state and input signals should not be applied.

Switching Waveforms (continued)

Write Cycle No. 2 ($\overline{CE}$ Controlled)[13,17,18]



Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW)[18]



Truth Table

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	I/O's	Mode	Power
H	X	X	High Z	Deselect/Power-down	Standby (I_{SB})
L	H	L	Data Out	Read	Active (I_{CC})
L	L	X	Data In	Write	Active (I_{CC})
L	H	H	High Z	Selected, Outputs Disabled	Active (I_{CC})

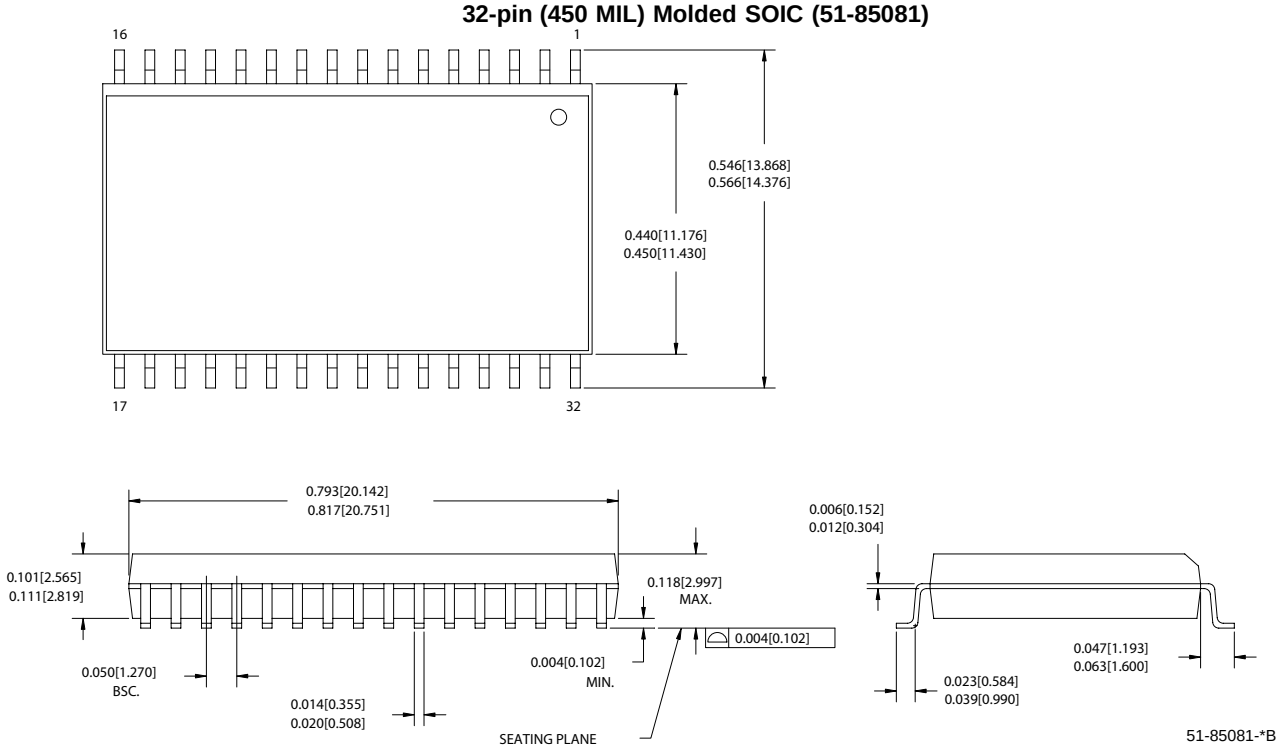
Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
45	CY62148ELL-45SXI	51-85081	32-pin Small Outline Integrated Circuit (Pb-Free)	Industrial
	CY62148ELL-45ZSXI	51-85095	32-pin Thin Small Outline Package II (Pb-Free)	
55	CY62148ELL-55SXE	51-85081	32-pin Small Outline Integrated Circuit (Pb-Free)	Automotive
	CY62148ELL-55ZSXE	51-85095	32-pin Thin Small Outline Package II (Pb-Free)	

Please contact your local Cypress sales representative for availability of these parts

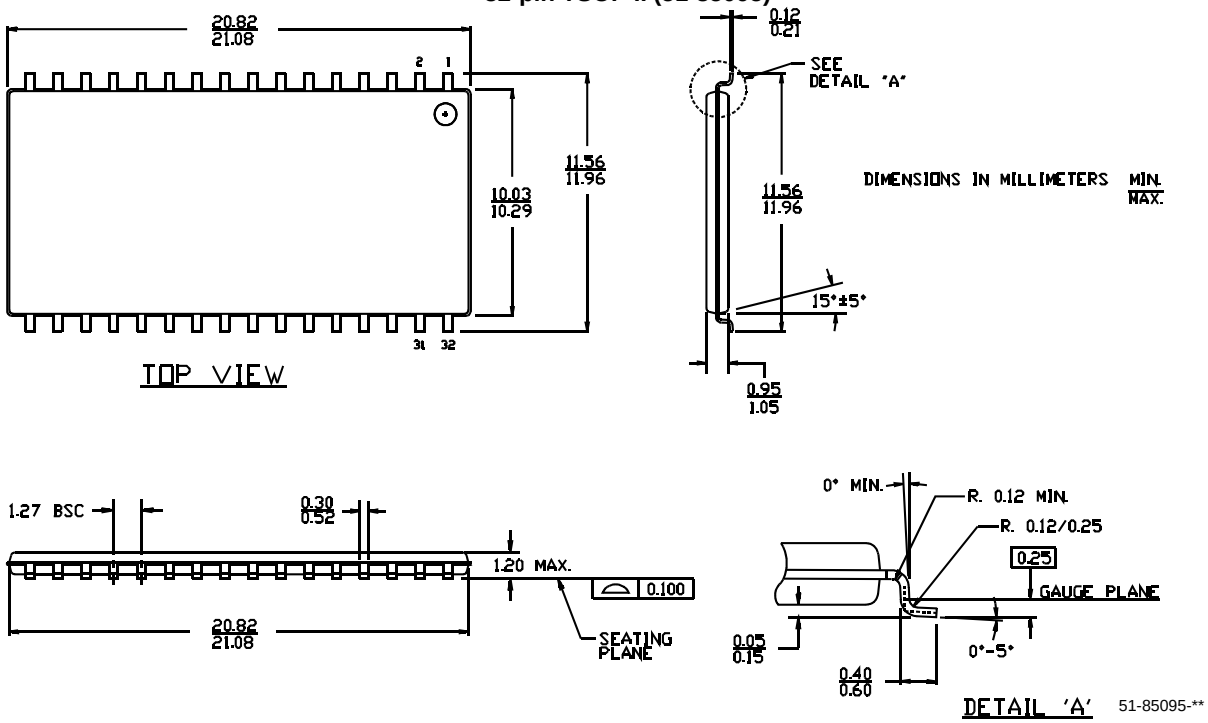
Package Diagrams

32-pin (450 MIL) Molded SOIC (51-85081)



Package Diagrams (continued)

32-pin TSOP II (51-85095)



Document History Page

Document Title: CY62148E MoBL® 4-Mbit (512K x 8) Static RAM Document Number: 38-05442				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	201580	01/08/04	AJU	New Data Sheet
*A	249276	See ECN	SYT	Changed from Advance Information to Preliminary Moved Product Portfolio to Page 2 Added RTSOP II and Removed FBGA Package Changed V_{CC} stabilization time in footnote #7 from 100 μs to 200 μs Changed I_{CCDR} from 2.0 μA to 2.5 μA Changed typo in Data Retention Characteristics(t_R) from 100 μs to t_{RC} ns Changed t_{OHA} from 6 ns to 10 ns for both 35 ns and 45 ns Speed Bin Changed t_{HZOE}, t_{HZWE} from 12 to 15 ns for 35 ns Speed Bin and 15 to 18 ns for 45 ns Speed Bin Changed t_{SCE} from 25 to 30 ns for 35 ns Speed Bin and 40 to 35 ns for 45 ns Speed Bin Changed t_{HZCE} from 12 to18 ns for 35 ns Speed Bin and 15 to 22 ns for 45 ns Speed Bin Changed t_{SD} from 15 to 18 ns for 35 ns Speed Bin and 20 to 22 ns for 45 ns Speed Bin Changed t_{DOE} from 15 to 18 ns for 35 ns Speed Bin Corrected typo in Package Name Changed Ordering Information to include Pb-Free Packages
*B	414820	See ECN	ZSD	Changed from Preliminary to Final Changed the address of Cypress Semiconductor Corporation on Page #1 from “3901 North First Street” to “198 Champion Court” Removed 35ns Speed Bin Removed “L” version of CY62148E Changed I_{CC} (Typ) value from 1.5 mA to 2 mA at f=1 MHz Changed I_{CC} (Max) value from 2 mA to 2.5 mA at f=1 MHz Changed I_{CC} (Typ) value from 12 mA to 15 mA at f=f_{max} Removed I_{SB1} spec from the Electrical characteristics table Changed I_{SB2} Typ. values from 0.7 μA to 1 μA and Max. values from 2.5 μA to 7 μA Modified footnote #4 to include current limit Removed redundant footnote on DNU pins Changed the AC testload capacitance from 100 pF to 30 pF on page #4 Changed test load parameters R1, R2, R_{TH} and V_{TH} from 1838 Ω, 994 Ω, 645 Ω and 1.75V to 1800 Ω, 990 Ω, 639 Ω and 1.77V Changed I_{CCDR} from 2.5 μA to 7 μA Added I_{CCDR} typical value Changed t_{LZOE} from 3 ns to 5 ns Changed t_{LZCE} and t_{LZWE} from 6 ns to 10 ns Changed t_{HZCE} from 22 ns to 18 ns Changed t_{PWE} from 30 ns to 35 ns Changed t_{SD} from 22 ns to 25 ns Updated the ordering information table and replaced Package Name column with Package Diagram
*C	464503	See ECN	NXR	Included Automotive Range in product offering Updated the Ordering Information
*D	485639	See ECN	VKN	Corrected the operating range to 4.5V - 5.5V on page# 3